

Atty. Dkt. No. 039153-0363 (F0804)

This listing of claims will replace all prior versions, and listings, of claims in the application:

## Listing of Claims:

1 1. (Currently Amended) A method of manufacturing an integrated circuit having  
2 a T-shaped gate conductor, the method comprising:

3 providing a gate dielectric layer above a top surface of a substrate;

4 providing a silicon and nitrogen containing layer above the gate dielectric  
5 layer;

6 providing an oxide layer above the silicon and nitrogen containing layer;

7 selectively etching the oxide layer to form a first trench in the oxide layer;

8 selectively etching the silicon and nitrogen containing layer to form a second  
9 trench in the silicon and nitrogen containing layer, the second trench being narrower than the  
10 first trench and being disposed below the first trench; and

11 providing a gate conductor material in the first trench and the second trench to  
12 form the T-shaped gate conductor.

1 2. (Original ) The method of claim 1, further comprising removing the oxide  
2 layer.

1 3. (Original ) The method of claim 2, further comprising:  
2 removing portions of the silicon and nitrogen containing layer, whereby a pair  
3 of spacers remain underneath the gate conductor material in the first trench.

1 4. (Original ) The method of claim 3, wherein the gate conductor material is  
2 removed by a polishing process.

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1           5.       (Original ) The method of claim 3, wherein the silicon and nitrogen containing  
2 layer includes silicon rich nitride.

1           6.       (Currently Amended) The method of claim 1, wherein the selective etching the  
2 silicon and nitrogen containing layer includes a selective etching and RELACS process.

1           7.       (Original ) The method of claim 1, wherein the silicon and nitrogen containing  
2 layer includes SiON or silicon rich nitride.

1           8.       (Original ) The method of claim 7, wherein the silicon and nitrogen containing  
2 layer is a silicon rich nitride layer.

1           9.       (Original ) The method of claim 1, wherein a width of the first trench is at  
2 least 250 Å and less than 1600 Å.

1           10.      (Original ) The method of claim 9, wherein the width of the second trench is at  
2 least 400 Å and less than 2100 Å.

1           11.      (Currently Amended) A method of manufacturing an ultra-large scale  
2 integrated circuit including a transistor with a T-shaped gate conductor, the method includes  
3 steps of:

4                   providing a first layer above a substrate, the first containing silicon and  
5 nitrogen;

6                   providing an oxide layer over the first layer;

7                   ~~forming~~ selectively etching a first trench in the oxide layer by etching;

8                   ~~forming~~ selectively etching a second trench by etching in the first layer, the  
9 second trench having a smaller width than the first trench; and

10                  providing a gate conductor material in the first trench and in the second trench  
11 to form the T-shaped gate conductor.

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1 12. (Original ) The method of claim 11, further comprising removing the oxide  
2 layer.

1 13. (Original ) The method of claim 12, further comprising removing portions of  
2 the first layer to leave spacers underneath the gate conductor material in the first trench, the  
3 removal process utilizing the gate conductor material as a mask.

1 14. (Original ) The method of claim 13, wherein the first layer is silicon rich  
2 nitride.

1 15. (Currently Amended) A method of manufacturing a T-shaped gate conductor  
2 for an integrated circuit, the method comprising:

3 providing a first layer above a gate dielectric layer, the gate dielectric layer  
4 being above a substrate, the first layer including silicon and nitrogen;

5 providing a second layer above the first layer;

6 selectively etching forming a first aperture in the second layer by etching;

7 selectively etching forming a second aperture in the first layer utilizing an  
8 etching process the second aperture being narrower than the first aperture;

9 filling the first aperture and the second aperture with a gate conductor  
10 material; and

11 removing the gate conductor material above the second layer, thereby leaving  
12 the T-shaped gate conductor in the first and second aperture.

1 16. (Previously Amended) The method of claim 15, wherein:  
2 the second layer is an oxide layer.

1 17. (Original ) The method of claim 16, wherein the gate conductor material is  
2 doped or undoped polysilicon material.

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1 18. (Previously Amended) The method of claim 17, wherein etching the second  
2 aperture uses a RELACS process.

1 19. (Previously Amended) The method of claim 16, wherein the gate conductor  
2 material is silicided.

1 20. (Original ) The method of claim 16, wherein the oxide layer is silicon dioxide.

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